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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,536	01/20/2004	Atsuhiro Yamashita	70366-011	7109

7590 07/09/2008
MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
ABDULSELAM, ABBAS I	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
07/09/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Office Action Summary	Application No.	Applicant(s)	
	10/759,536	YAMASHITA ET AL.	
	Examiner	Art Unit	
	ABBAS I. ABDULSELAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. This office action is in response to a communication filed on 05/19/2008. Claims 3-28 are pending, and claims 1-2 are canceled.

2. Applicant's arguments filed on 05/19/2008 have been fully considered but they are not persuasive.

With respect to claim 9, applicant argues, a previous rejection made based on 35 USC 112 second paragraphs.

In response, the examiner withdraws the 112 second paragraph rejection on claim 9.

On pages 18-19 of applicant's "REMARKS", applicant lisSt all claim limitations of claim 3, and argues that the cited reference Kitai et al. (USPN 7133009) does not teach a claim limitation "control means for controlling the timing of the on-operation of the on -control element or the off-operation of the off-control element in a accordance with the output voltage of the voltage holding means".

The examiner disagrees with the applicant's argument. As shown in the rejection below, Kitai teaches as shown in the art ejection below, a switching medium 34 is incorporated within each capacitively switched pixel (45) below the associated row electrode such that if the difference in voltage between the electrodes is 25 volts or less, the medium 34 is an insulator, if this voltage difference rises above 25 volts, the medium 34 becomes conductive, but it again becomes insulating if the voltage difference subsequently falls below 25 volts, (Fig. 5a (34), col. 6, lines 41-46, col. 7, lines 5-15, col. 8, lines 36-42. Note that the status of switching medium 34

being an insulating capacitive and then being conductive corresponds to switched pixel 45 being turn "off" and 'on" as evidenced in the introduction(col. 2, lines 40-44). Kitai teaches charging time constant of columns enabling a higher refresh rate for the entire display. Kitai also teaches circuit associated with a switchable pixel 45 enables to alter the time needed to charge and discharge the EL capacitance structure (col. 9, lines 48-67, col. 10, lines 1-4). Note that as shown in Fig. 6b, in order for medium 34 to be conductive, a charge has to flow into the inner electrode 52. Hence, clearly, the configuration of the switching medium 34, which can be switched between a state in which it functions as a capacitor and a state it functions as a conductor reads on the claimed "control means".

On page 19-22 of applicant's "REMARKS", and with respect to claims 4-5, applicant lists all claim limitations of claims 4-5, and repeated the same argument by stating that Kitai's switching medium does not control the timing of the on-operation of the on-control element or the off-operation of the off-control element in accordance with the output voltage of the voltage holding means .Applicant also argues that Kitai does not teach an off-control element for each pixel and on-control element for each pixel.

The examiner disagrees with the applicant's argument. As stated above , Kitai teaches a switching medium 34, which could be an insulating capacitive and then conductive that corresponds to switched pixel 45 being turn "off" and 'on" as evidenced in the introduction (col. 2, lines 40-44). Kitai teaches charging time constant of columns enabling a higher refresh rate for the entire display. Kitai also teaches circuit associated with a switchable pixel 45 enables to alter the time needed to charge and discharge the EL capacitance structure (col. 9, lines 48-51-67, col. 10, lines 1-4). Note that as shown in Fig. 6b, in order for medium 34 to be conductive, a charge

has to flow into the inner electrode 52. Hence, clearly, the configuration of the switching medium 34, which can be switched between a state in which it functions as a capacitor and a state it functions as a conductor reads on the argued claimed limitation.

On page 22-23 of applicant's "REMARKS", applicant lists all claim limitations of claims 11 and argues that Kitai does not teach " the control circuit of each pixel of the display panel comprises a first control element for starting to energize the display element and a second control element for deenergizing the display element".

The examiner disagrees with the applicant's argument. As shown in the rejection below, Kitai teaches a circuit element (34) which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor depending on the voltage applied across the circuit element; for example, if the difference in voltage between the electrodes is 25 volts or less, the medium 34 is an insulator, if this voltage difference rises above 25 volts, the medium 34 becomes conductive, but it again becomes insulating if the voltage difference subsequently falls below 25 volts((Fig. 5a (34), col. 6, lines 41-46, col. 7, lines 5-15). Hence it is clear that the same medium 34 serves to read over the claimed "first control element and second control element. Note that claim 11 does not say two *separate* control elements as applicant alleges.

Applicant also argues with respect to claim 11, Kitai does not teach "the first control element is provided on and connected in series with a power supply line extending from a power source for supplying the electric power to the display element, is turned on when starting to energize the display element and starts to energize the display element, and the second control

element is turned on when deenergizing the display element and turns off the first control element to thereby deenergize the display element".

The examiner disagrees with the applicant's argument. As shown in the art rejection below, Kitai teaches a circuit element which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor depending on the voltage applied across the circuit element; for example, if the difference in voltage between the electrodes is 25 volts or less, the medium 34 is an insulator, if this voltage difference rises above 25 volts, the medium 34 becomes conductive, but it again becomes insulating if the voltage difference subsequently falls below 25 volts (Fig. 5a (34), col. 6, lines 41-46, col. 7, lines 5-15, note that power supply means is connected the array of matrix addressed capacitively switchable electroluminescent pixels for providing power to each capacitively switchable electroluminescent pixel, and the switching medium 34 is incorporated within each capacitively switched pixel (45) below the associated row electrode (col. 5, lines 31-34, col. 8, lines 36-42).

On page 24-26 of applicant's "REMARKS", applicant lists all claim limitations of claim 6, and argues that the cited references Kitai et al. (USPN 7133009) in view of Graves (USPN 4554539) do not teach pulse-width modulation control means for on/off-controlling the drive element.

The examiner disagrees with the applicant's argument.

As mentioned above, while kitai teaches switching medium 34, which is incorporated within each capacitively switched pixel (45) below the associated row electrode such that if the

difference in voltage between the electrodes is 25 volts or less, the medium 34 is an insulator, if this voltage difference rises above 25 volts, the medium 34 becomes conductive,

Kitai does not teach pulse-width modulation control means for on/off-controlling the drive element.

Graves illustrates a desired brightness information for any individual pixel location is presented to a column driver as a logic level pulse-positioned modulated (PPM) or pulse-width modulated (PWM) signal 24, such that the column driver output is switched from low to high (HV1 level) by the pulse modulated information using the level shifter 26 in a switching mode (Fig. 5 (24, 26), Fig. 2 (24, column, drivers), col. 3, lines 41-49). Graves further teaches the pixel's row driver is source (NFETS with negative select voltage) driven with a ramped voltage so that the peak applied differential voltage at the selected pixel (and therefore its brightness) is a function of the pulse modulated information such that The term " ramped voltage" is intended to apply to any voltage which varies with time including a stair-stepped voltage (col. 3, lines 41-49 and col. 4, lines 63-65).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kitai's matrix addressed EL display shown in Fig. 6a including a switching medium 34 with Graves column driver (which receives as a logic level pulse-positioned modulated (PPM) or pulse-width modulated (PWM) signal 24) as configured in Fig. 2, because the use of a column driver with pulse-width modulation helps an electroluminescent display dissipate low power as taught by Graves (col. 2, lines 21-23, col. 2, lines 31-37).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on

combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

On page 26-27 of applicant's "REMARKS", Applicant lists all clam limitations of claim 28 and argues the following:

"Graves does not disclose the claimed capacitor. Therefore, the reference cannot suggest supplying the drive transistor with the sum of ram voltage and the output voltage of the capacitor. Kitani does not disclose the ram voltage. Therefore, this reference also cannot suggest supplying the drive transistor with the sum of ram voltage and the output voltage of the capacitor"

The examiner disagrees with the applicant's argument. As shown in the ejection below,

Kitani teaches a circuit element (switching medium) 34 which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor depending on the voltage applied across the circuit element (Fig. 5a (34), col. 6, lines 41-46, col. 7, lines 5-1).

Kitai does not teach a voltage in accordance with the sum of ramp voltage having a predetermined rate of variation.

Graves illustrates desired brightness information for any individual pixel location is presented to a column driver as logic level pulse-positioned modulated (PPM) or pulse-width modulated (PWM) signal 24. Graves further teaches the pixel's row driver is source (NFETS with negative select voltage) driven with a ramped voltage so that the peak applied differential voltage at the selected pixel (and therefore its brightness) is a function of the pulse modulated information such that the term " ramped voltage" is intended to apply to any voltage which varies

with time including a stair-stepped voltage, and column (col. 3, lines 41-49 and col. 4, lines 63-65). Graves teaches as explained in abstract, a circuit operates in a switching mode, and has a row driver which switches a timed ramp voltage to a selected row of the display. Graves teaches the use of drive transistor as switches (col. 4, lines 3-4), note that application of voltage to the gate of a transistor is well known.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kitani's matrix addressed EL display shown in Fig. 6a including a switching medium 34, which serves as a capacitor with Graves column driver (which receives as a logic level pulse-positioned modulated (PPM) or pulse-width modulated (PWM) signal 24) along with ramped voltage as configured in Fig. 2, because the use of a column driver with pulse-width modulation helps an electroluminescent display dissipate low power as taught by Graves (col. 2, lines 21-23, col. 2, lines 31-37).

Note that with respect to claim limitation "the output voltage of the capacitor is applied to the gate of the drive transistor", Kitani in view of Graves teaches a switching medium 34, which serves as a capacitor. Hence, one of ordinary skill would have ascertained that it would be obvious to manipulate Kitani's modified medium 34 in a desired input-output mechanism.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

On page 26-27 of applicant's "REMARKS", applicant argues that dependent claims 7-10, 12-19 and 22-27 are defined over the prior art in connection with their respective independent claims.

The examiner disagrees with the applicant's argument for the reasons set forth in response to argument with respect the independent claims.

Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 3-5, 11 and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Kitai et al. (USPN 7133009).

Regarding claim 3 , Kitai teaches a display device of the active matrix drive type comprising a display panel having a plurality of pixels arranged in the form of a matrix, and a scanning driver and a data driver which are connected to the display panel, the display device being characterized in that each of the pixels of the display panel comprises a display element luminescent when supplied with current or voltage, a write element to be brought into conduction when impressed with scanning voltage from the scanning driver***(Fig. 6a, Fig. 6b (45), EL (45), a matrix addressed EL display including a switchable EL pixel (45), col. 7, lines***

21-26, Fig. 5b, current voltage characteristics, col. 7, lines 62-66, note that at higher voltages, a switching material 34 becomes conductive and charge flows into inner electrode 52, and it is inherent that column electrodes and row electrodes shown in Fig. 6a have their corresponding drivers), voltage holding means to be impressed with data voltage from the data driver by the conduction of the write element for holding the data voltage ***(col. 5, lines 42-45, col. 7, lines 60-62, the capacitively switched circuit element may be a solid state dielectric which functions as a capacitor in a selected voltage range such that the capacitance is partly defined by the switching material 34)***, a drive element for energizing or deenergizing the display element in response to the input of an on/off control signal, an on-control element for turning on the drive element, an off-control element for turning off the drive element, and control means for controlling the timing of the on-operation of the on-control element or the off-operation of the off-control element in accordance with the output voltage of the voltage holding means ***(Fig. 5a (34), col. 6, lines 41-46, col. 7, lines 5-15, col. 8, lines 52-67, a circuit element which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor depending on the voltage applied across the circuit element; for example, if the difference in voltage between the electrodes is 25 volts or less, the medium 34 is an insulator, if this voltage difference rises above 25 volts, the medium 34 becomes conductive, but it again becomes insulating if the voltage difference subsequently falls below 25 volts, col. 8, lines 36-42, note that the switching medium 34 is incorporated within each capacitively switched pixel (45) below the associated row electrode 54, col. 6, lines 41-46, col. 9, lines 62-67the presence of the circuit elements result in reduction of time needed to charge and discharge EL capacitance structure).***

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Regarding claim 4, Kitai teaches a display device of the active matrix drive type comprising a display panel having a plurality of pixels arranged in the form of a matrix, and a scanning driver and a data driver which are connected to the display panel, the display device being characterized in that each of the pixels of the display panel comprises a display element luminescent when supplied with current or voltage***(Fig. 6a, Fig. 6b (45), EL (45), a matrix addressed EL display including a switchable EL pixel (45), col. 7, lines 21-26, Fig. 5b, current voltage characteristics, it is inherent that column electrodes and row electrodes shown in Fig. 6a have their corresponding drivers)***, a write element to be brought into conduction when impressed with scanning voltage from the scanning driver, voltage holding means to be impressed with data voltage from the data driver by the conduction of the write element for holding the data voltage ***(col. 7, lines 62-66, note that at higher voltages, a switching material 34 becomes conductive and charge flows into inner electrode 52, it is inherent that column electrodes and row electrodes shown in Fig. 6a have their corresponding drivers, col. 5, lines 42-45, col. 7, lines 60-62, the capacitively switched circuit element may be a solid state dielectric which functions as a capacitor in a selected voltage range such that the capacitance is partly defined by the switching material 34)***, a drive element for energizing or deenergizing the display element in response to the input of an on/off control signal and an off-control element for turning off the drive element, the pixels being divided into pixel groups each comprising pixels adjacent to one another and each having an on-control element for turning on the drive element of each of the pixels of the group, and control means for controlling the timing of the

off-operation of the off-control element in accordance with the output voltage of the voltage holding means of each pixel***(Fig. 5a (34), col. 6, lines 41-46, col. 7, lines 5-15, col. 8, lines 52-67, a circuit element which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor depending on the voltage applied across the circuit element; for example, if the difference in voltage between the electrodes is 25 volts or less, the medium 34 is an insulator, if this voltage difference rises above 25 volts, the medium 34 becomes conductive, but it again becomes insulating if the voltage difference subsequently falls below 25 volts, col. 8, lines 36-42, note that the switching medium 34 is incorporated within each capacitively switched pixel (45) below the associated row electrode 54, note that the display includes an array of matrix addressed capacitively switchable electroluminescent pixels each capacitively switchable electroluminescent pixel including an electroluminescent pixel and a circuit element, col. 6, lines 41-46, col. 9, lines 62-67, the presence of the circuit elements result in reduction of time needed to charge and discharge EL capacitance structure).***

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Regarding claim 5, Kitai teaches a display device of the active matrix drive type comprising a display panel having a plurality of pixels arranged in the form of a matrix, and a scanning driver and a data driver which are connected to the display panel, the display device being characterized in that each of the pixels of the display panel comprises a display element luminescent when supplied with current or voltage***(Fig. 6a, Fig. 6b (45), EL (45), a matrix addressed EL display including a switchable EL pixel, col. 7, lines 21-26, Fig. 5b, current voltage characteristics, it is inherent that column electrodes and row electrodes shown in Fig.***

6a have their corresponding drivers), a write element to be brought into conduction when impressed with scanning voltage from the scanning driver, voltage holding means to be impressed with data voltage from the data driver by the conduction of the write element for holding the data voltage ***(col. 7, lines 62-66, note that at higher voltages, a switching material 34 becomes conductive and charge flows into inner electrode 52, it is inherent that column electrodes and row electrodes shown in Fig. 6a have their corresponding drivers, col. 5, lines 42-45, col. 7, lines 60-62, the capacitively switched circuit element may be a solid state dielectric which functions as a capacitor in a selected voltage range such that the capacitance is partly defined by the switching material 34)***, a drive element for energizing or deenergizing the display element in response to the input of an on/off control signal and an on-control element for turning on the drive element, the pixels being divided into pixel groups each comprising pixels adjacent to one another and each having an off-control element for turning off the drive element of each of the pixels of the group, and control means for controlling the timing of the on-operation of the on-control element in accordance with the output voltage of the voltage holding means of each pixel***(Fig. 5a (34), col. 6, lines 41-46, col. 7, lines 5-15, col. 8, lines 52-67, a circuit element which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor depending on the voltage applied across the circuit element; for example, if the difference in voltage between the electrodes is 25 volts or less, the medium 34 is an insulator, if this voltage difference rises above 25 volts, the medium 34 becomes conductive, but it again becomes insulating if the voltage difference subsequently falls below 25 volts, col. 8, lines 36-42, note that the switching medium 34 is incorporated within each capacitively switched pixel (45) below the associated row electrode***

54, note that the display includes an array of matrix addressed capacitively switchable electroluminescent pixels each capacitively switchable electroluminescent pixel including an electroluminescent pixel and a circuit element, col. 6, lines 41-46, col. 9, lines 62-67, the presence of the circuit elements result in reduction of time needed to charge and discharge EL capacitance structure).

Regarding claim 11, and 20-21, Regarding claim 1, Kitai teaches a display device of the active matrix drive type comprising a display panel having a plurality of pixels arranged in the form of a matrix, each of the pixels of the display panel having a display element luminescent when supplied with electric power ***(Fig. 6a, Fig. 6b (45), EL (45), a matrix addressed EL display including a switchable EL pixel, col. 7, lines 21-26, Fig. 5b, current voltage characteristics)***, and a control circuit for controlling the luminescence period of the display element within 1 frame period in accordance with data voltage to be supplied from outside ***(col. 6, lines 41-46, col. 9, lines 62-67, incorporates into each EL pixel at least one circuit element which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor depending on the voltage applied across the circuit element, such that the presence of the circuit elements result in reduction of time needed to charge and discharge EL capacitance structure)***, the display device being characterized in that the control circuit of each pixel of the display panel comprises a first control element for starting to energize the display element and a second control element for deenergizing the display element ***(Fig. 5a (34), col. 6, lines 41-46, col. 7, lines 5-15, a circuit element which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor***

depending on the voltage applied across the circuit element; for example, if the difference in voltage between the electrodes is 25 volts or less, the medium 34 is an insulator, if this voltage difference rises above 25 volts, the medium 34 becomes conductive, but it again becomes insulating if the voltage difference subsequently falls below 25 volts), wherein the first control element is provided on and connected in series with a power supply line extending from a power source for supplying the electric power to the display element, is turned on when starting to energize the display element and starts to energize the display element, and the second control element is turned on when deenergizing the display element and turns off the first control element to thereby deenergize the display element ***(Fig. 5a (34), col. 6, lines 41-46, col. 7, lines 5-15, a circuit element which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor depending on the voltage applied across the circuit element; for example, if the difference in voltage between the electrodes is 25 volts or less, the medium 34 is an insulator, if this voltage difference rises above 25 volts, the medium 34 becomes conductive, but it again becomes insulating if the voltage difference subsequently falls below 25 volts, col. 5, lines 31-34, col. 8, lines 36-42, note that power supply means is connected the array of matrix addressed capacitively switchable electroluminescent pixels for providing power to each capacitively switchable electroluminescent pixel, and the switching medium 34 is incorporated within each capacitively switched pixel (45) below the associated row electrode 54).***

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6-8, 12-19 and 22-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitai et al. (USPN 7133009) in view of Graves (USPN 4554539).

Regarding claim 28, Kitai teaches a display device of the active matrix drive type comprising a display panel having a plurality of pixels arranged in the form of a matrix, each of the pixels of the display panel having a display element luminescent when supplied with electric power ***(Fig. 6a, Fig. 6b (45), EL (45), a matrix addressed EL display including a switchable EL pixel, col. 7, lines 21-26, Fig. 5b, current voltage characteristics)***, and a control circuit for controlling the luminescence period of the display element within 1 frame period in accordance with data voltage to be supplied from outside ***(col. 6, lines 41-46, col. 9, lines 62-67, incorporates into each EL pixel at least one circuit element which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor depending on the voltage applied across the circuit element, such that the presence of the circuit elements result in reduction of time needed to charge and discharge EL capacitance structure)***, the display device being characterized in that the control circuit of each pixel of the display panel has a write transistor to be brought into conduction when impressed with scanning voltage, a capacitor to be impressed with data voltage by the conduction of the write transistor for holding the data voltage ***(Fig. 5a (34), col. 6, lines 41-46, col. 7, lines 5-15, a circuit element***

which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor depending on the voltage applied across the circuit element; for example, if the difference in voltage between the electrodes is 25 volts or less, the medium 34 is an insulator, if this voltage difference rises above 25 volts, the medium 34 becomes conductive, but it again becomes insulating if the voltage difference subsequently falls below 25 volt, it is apparent that that EL pixel has to a have a transistor to functions).

, and a drive transistor provided on and connected in series with a power supply line for supplying the electric power to the display element and to be brought into conduction upon the difference between the voltage to be applied to a gate thereof and the voltage at one terminal of the display element exceeding a predetermined threshold value, ***(col. 8, lines 36-42, note that power supply means is connected the array of matrix addressed capacitively switchable electroluminescent pixels for providing power to each capacitively switchable electroluminescent pixel, and the switching medium 34 is incorporated within each capacitively switched pixel (45) below the associated row electrode 54, it is apparent that that EL pixel has to a have a transistor to function col. 6, lines 46-49, below threshold voltage the circuit element is in the capacitive state and in the conducting state when voltages above the threshold are applied, note that it is apparent that that each EL pixel has to a have a transistor to function, and the application of gate voltages is well know).***

Kitai does not teach a voltage in accordance with the sum of ramp voltage having a predetermined rate of variation and the output voltage of the capacitor is applied to the gate of the drive transistor.

Graves illustrates desired brightness information for any individual pixel location is presented to a column driver as logic level pulse-positioned modulated (PPM) or pulse-width modulated (PWM) signal 24. Graves further teaches the pixel's row driver is source (NFETS with negative select voltage) driven with a ramped voltage so that the peak applied differential voltage at the selected pixel (and therefore its brightness) is a function of the pulse modulated information such that the term " ramped voltage" is intended to apply to any voltage which varies with time including a stair-stepped voltage, and column (col. 3, lines 41-49 and col. 4, lines 63-65). Graves teaches as explained in abstract, a circuit operates in a switching mode, and has a row driver which switches a timed ramp voltage to a selected row of the display. Graves teaches the use of drive transistor as switches (col. 4, lines 3-4), note that application of voltage to the gate of a transistor is well known.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kitai's matrix addressed EL display shown in Fig. 6a with Graves column driver (which receives as a logic level pulse-positioned modulated (PPM) or pulse-width modulated (PWM) signal 24) along with ramped voltage as configured in Fig. 2, because the use of a column driver with pulse-width modulation helps an electroluminescent display dissipate low power as taught by Graves (col. 2, lines 21-23, col. 2, lines 31-37).

Regarding claims 13-19 and 22-27, Kitai teaches the control circuit of each pixel of the display panel has a write transistor to be brought into conduction when impressed with scanning voltage and a capacitor to be impressed with data voltage by the conduction of the write

transistor for holding ***the data voltage(Fig. 6a, Fig. 6b (45), EL (45), col. 8, lines 40-42, a matrix addressed EL display including a capacitively switchable EL pixel (45) such that each capacitively switched EL pixel incorporates element which can be switched between a state in which it functions as a capacitor and a state in which it functions as a conductor, col. 7, lines 21-26, Fig. 5b, current voltage characteristics, col. 7, lines 62-66, note that at higher voltages, a switching material 34 becomes conductive and charge flows into inner electrode 52, and it is inherent that column electrodes and row electrodes shown in Fig. 6a have their corresponding drivers, also it is apparent that that EL pixel has to a have a transistor to function)***, the first control element comprising a first transistor provided on and connected in series with the power supply line ***(col. 8, lines 36-42, note that power supply means is connected the array of matrix addressed capacitively switchable electroluminescent pixels for providing power to each capacitively switchable electroluminescent pixel, and the switching medium 34 is incorporated within each capacitively switched pixel (45) below the associated row electrode 54, it is apparent that that EL pixel has to a have a transistor to function)*** and to be brought into conduction upon the difference between the voltage to be applied to a gate thereof and the voltage of the power source exceeding a predetermined threshold value, the second control element comprising a second transistor to be brought into conduction upon the difference between the voltage to be applied to a gate thereof and the power source voltage exceeding a predetermined threshold value to bring the first transistor out of conduction ***(col. 6, lines 46-49, below threshold voltage the circuit element is in the capacitive state and in the conducting state when voltages above the threshold are applied, col. 10, lines 5-14, capacitive switching in***

terms of bi-directional diodes, note that it is apparent that that each EL pixel has to a have a transistor to function, and the application of gate voltages is well known).

Kitai does not teach a voltage in accordance with the sum of a first ramp voltage having a predetermined rate of variation and the output voltage of the capacitor is applied to the gate of the first transistor, and a second ramp voltage having a predetermined rate of variation is applied to the gate of the second transistor.

Graves illustrates desired brightness information for any individual pixel location is presented to a column driver as logic level pulse-positioned modulated (PPM) or pulse-width modulated (PWM) signal 24. Graves further teaches the pixel's row driver is source (NFETS with negative select voltage) driven with a ramped voltage so that the peak applied differential voltage at the selected pixel (and therefore its brightness) is a function of the pulse modulated information such that the term " ramped voltage" is intended to apply to any voltage which varies with time including a stair-stepped voltage, and column (col. 3, lines 41-49 and col. 4, lines 63-65). Graves teaches as explained in abstract, a circuit operates in a switching mode, and has a row driver which switches a timed ramp voltage to a selected row of the display. Graves teaches the use of drive transistor as switches (col. 4, lines 3-4), note that application of voltage to the gate of a transistor is well known.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kitai's matrix addressed EL display shown in Fig. 6a with Graves column driver (which receives as a logic level pulse-positioned modulated (PPM) or

pulse-width modulated (PWM) signal 24) along with ramped voltage as configured in Fig. 2, because the use of a column driver with pulse-width modulation helps an electroluminescent display dissipate low power as taught by Graves (col. 2, lines 21-23, col. 2, lines 31-37).

Regarding claim 6, Kitai teaches a display device of the active matrix drive type comprising a display panel having a plurality of pixels arranged in the form of a matrix, and a scanning driver and a data driver which are connected to the display panel, the display device being characterized in that each of the pixels of the display panel comprises: a display element luminescent when supplied with current or voltage***(Fig. 6a, Fig. 6b (45), EL (45), a matrix addressed EL display including a switchable EL pixel, col. 7, lines 21-26, Fig. 5b, current voltage characteristics, it is inherent that column electrodes and row electrodes shown in Fig. 6a have their corresponding drivers)***, a write element to be brought into conduction when impressed with scanning voltage from the scanning driver, voltage holding means to be impressed with data voltage from the data driver by the conduction of the write element for holding the data voltage***(col. 7, lines 62-66, note that at higher voltages, a switching material 34 becomes conductive and charge flows into inner electrode 52, it is inherent that column electrodes and row electrodes shown in Fig. 6a have their corresponding drivers, col. 5, lines 42-45, col. 7, lines 60-62, the capacitively switched circuit element may be a solid state dielectric which functions as a capacitor in a selected voltage range such that the capacitance is partly defined by the switching material 34)***, a drive element for energizing or deenergizing the display element in response to the input of an on/off control signal ***(Fig. 5a (34), col. 6, lines 41-46, col. 7, lines 5-15, col. 8, lines 52-67, a circuit element which can be switched between a***

state in which it functions as a capacitor and a state in which it functions as a conductor depending on the voltage applied across the circuit element; for example, if the difference in voltage between the electrodes is 25 volts or less, the medium 34 is an insulator, if this voltage difference rises above 25 volts, the medium 34 becomes conductive, but it again becomes insulating if the voltage difference subsequently falls below 25 volts),

Kitai does not teach pulse-width modulation control means for on/off-controlling the drive element by pulse-width-modulating the output voltage of the voltage holding means with ramp voltage having a predetermined rate of variation, the pulse-width modulation control means comprising an on-control element for turning on the drive element, and an off-control element for turning off the drive element.

Graves illustrates a desired brightness information for any individual pixel location is presented to a column driver as a logic level pulse-positioned modulated (PPM) or pulse-width modulated (PWM) signal 24, such that the column driver output is switched from low to high (HV1 level) by the pulse modulated information using the level shifter 26 in a switching mode (Fig. 5 (24, 26), Fig. 2 (24, column, drivers), col. 3, lines 41-49). Graves further teaches the pixel's row driver is source (NFETS with negative select voltage) driven with a ramped voltage so that the peak applied differential voltage at the selected pixel (and therefore its brightness) is a function of the pulse modulated information such that The term " ramped voltage" is intended to apply to any voltage which varies with time including a stair-stepped voltage (col. 3, lines 41-49 and col. 4, lines 63-65).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kitai's matrix addressed EL display shown in Fig. 6a with Graves column driver (which receives as a logic level pulse-positioned modulated (PPM) or pulse-width modulated (PWM) signal 24) along with ramped voltage as configured in Fig. 2, because the use of a column driver with pulse-width modulation helps an electroluminescent display dissipate low power as taught by Graves (col. 2, lines 21-23, col. 2, lines 31-37).

Regarding claims 7-8, and 12, Graves teaches the on-control element operates when impressed with a voltage in accordance with the ramp voltage to turn on the drive element, and the off-control element operates when impressed with a voltage in accordance with the sum of the data voltage and the ramp voltage to turn off the drive element ***(Fig. 2 and the abstract, a circuit operates in a switching mode , and has a row driver which switches a timed ramp voltage to a selected row of the display. A column driver is used to switch selected columns from a low to a high voltage. The column driver is pulse-modulated (PPM or PWM) so that each pulse is timed to coincide with the ramped voltage to provide a differential voltage peak which provides the desired brightness (or grey scale) at the pixel where the driven row and column cross).***

7. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitai et al. (USPN 7133009) in view of Kasai (USPN 7012597).

Regarding claims 9-10, Kitai does not teach a signal line connecting a power source of high potential for supplying the current to the display element to a power source of a low potential serving as an operation reference for the on-control element and the off-control element has an element provided thereon for blocking the current flowing from the power source of high potential to the power source of low potential, and of the pixels of the display panel comprises a current program circuit for programming the current to be passed through the display element.

Kasai on the other illustrates as shown in Fig. 3, a power supply voltage, VDD, and a pixel circuit (200)(a current programming circuit), which includes switching transistors (211, 212, and a fourth transistor (214), which is a drive transistor for controlling the value of the current flowing in an organic electroluminescent device or luminescent element (220) (col. 4, lines 21-24, col. 4, lines 59-63). Kasai further teaches that the value of the current in the fourth transistor 214 is controlled by the amount of charge in the storage capacitor (230)(col. 4, lines 62-64, col. 4, lines 32-33). Note that as shown in Fig. 3, a power supply voltage, VDD (top) is connected to a ground (bottom) between which a storage capacitor (230) is located. Also, note that since the value of the current in the fourth transistor 214 is controlled by the amount of charge in the storage capacitor (230), one can halt the current the fourth transistor 214 by manipulating the amount of charge in the storage capacitor (230).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Kitai's EL pixel (45) shown in Fig. 6B with Kasai's pixel circuit (200) as configured in Fig. 3, because the use of a pixel circuit (200) helps regulate light emission level of an organic electroluminescent display system as taught by Kasai (col. 4, lines 21-25)

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is 571-272-7685.The examiner can normally be reached on Monday through Friday from 9:00A.M.to 5:30

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Abbas I Abdulselam/
Primary Examiner, Art Unit 2629
July 1, 2008